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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,567	10/08/2004	Hirohisa Miyazawa	029267.55488US	9020

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EXAMINER

DINH, TUAN T

ART UNIT	PAPER NUMBER
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2841

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04/06/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/510,567		MIYAZAWA, HIROHISA	
	Examiner		Art Unit	
	Tuan T. Dinh		2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09/01/09.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3 and 5-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>06/10/08</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. In view of the decision on appeal from Board of Patent Appeals and Interferences made on 09/01/09 based on Reply Brief filed on 09/24/08, a new ground of rejection is now made as set forth below. Although the board has reversed the examiner on the rejections previously set forth, examiner set forth a new ground of rejection based on prior arts known to the examiner which indicate the unpatentability of the appealed claims. The prior arts were previously cited to the applicant on 10/2/2006 and 4/30/2007. The primary reference in the rejection of Yasuho (U.S. Patent 6,303,989) was not used in the rejection before (only cited as related art to be made known to the applicant dated 10/2/2006.) The secondary references of Aruga et al. (U.S. Patent 6,085,137) and Yasuho (U.S. Patent 5,346,402) were used in the prior rejections for dependent claims. Prosecution is hereby reopened.

Noted in applicant's specification:

[0005] a plurality of low-frequency electronic components such as a power circuit, a gyro, a GPS circuit, and a plurality of high-frequency electronic components such as a CPU chip, a memory chip and a graphics chip.

Note of claimed language:

The term "**a high-speed module board**" is defined as a printed circuit board or PCB comprising plurality of high-speed components (microchips) mounted on the PCB

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(for example, a processor (CPU), memory or flash memory, DDR, DDR2 etc.), Google-Answer.com.

Claim Objections

2. Claims 5, 7-8 are objected to because of the following informalities:

Claim 5, line 4, please, change "a plurality of high frequency..." to - - the plurality of high frequency... - - for proper antecedence basis.

Claims 7-8, line 3, change "the four connector terminals" to - - the connector terminals having four connector terminals - - for proper antecedence basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Yasuho et al. (U.S. Patent 6,303,989) cited in the record, 10/12/2006.

As to claim 1, Yasuho ('989) discloses a circuit board device as shown in figures 1-2 comprising:

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a base board (**element 1**-figure 1, column 2, line 3, or **element 21**, column 3, line 10) having a plurality of low frequency electronic components (power supply such as **DC/DC or AC/DC converters 4**, column 2, lines 9-11, or power supply such as **DC/DC or AC/DC converters 22** column 3, line 14);

(The low frequency electronic component as described in the specification in Paragraph [0005] is **a power circuit**, the power supply or AC/DC converter is defined as an electronic circuit which converts one direct-current voltage into another, consisting of an inverter followed by a step-up or step-down transformer and rectifier. Thus, the power supply or converter is also a power circuit. Therefore, the converter is the low frequency component); and

a multilayer module board (**element 7**-figure 1, column 2, line 18) mounted at one surface (a top surface) of the base board (**1 or 21**) and having a plurality of high-frequency electronic components (**8, 10, 11, and 14**, see column 2, lines 24-36) including at least one CPU (**CPU-8**, column 2, line 24) and a plurality of memory chips (**cache memory 11 and 14 data buffer LSI**);

(Noted in the specification): the plurality of high-frequency electronic components are such as a CPU chip, a memory chip and a graphics chip (see paragraph [0005])

wherein

the multilayer module board (7) is one of:

a low-end module board, a high speed module board, or an advance function board;

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The multilayer module (7), which is the high-speed module board (see noted as above), connected on (the connection of the multilayer board to the base board by pins 5) the base board (1 or 21).

As to claim 5, Yasuho discloses the multilayer module board (7) comprising the plurality of high-frequency electronic components including a CPU (8) and a memory (11 and 14) mounted at (see claim 1), at least, a surface thereof, wherein:

the plurality of high-frequency electronic components (8, 10-11, 14) are electrically connected with one another through a wiring patterns (not shown) formed at an inner layer thereof (see column 1, lines 40-46).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: cited in the record 04/30/07

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuho ('989) in view of Aruga et al. (U.S. Patent 6,085,137) both references cited in the record 10/12/2006.

Regarding to claim 3, Yasuho discloses all of the limitations, except for the device being used in a navigation system.

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Aruga et al. teaches a vehicle control device (1) as shown in figure 1 comprising a navigation system (10) comprising at least a power circuit, a gyro and a GPS circuit are mounted at the base board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Aruga et al. employed in the device of Yasuho in order to provide information and detect road guide for the vehicle.

7. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuho ('989) in view Yasuho et al. (U.S. Patent 5,346,402) cited in the record 04/30/07.

Regarding claim 6 (claim 6 is depended on claim 5/1), Yasuho ('989) discloses the multilayer board (7) having shaped, which is a rectangular, except for:

connector terminals provided as separate members each soldered onto one of four peripheral edges thereof.

Yasuho et al. ('402) shows an insulating substrate (7) having connector terminals (4) provided as separate members each soldered onto one of four peripheral edges (edges of a frame 3 of the substrate 7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. (402) employed in the device of Yasuho ('989) in order to provide a high density electrical connection.

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Regarding claims 7 (claim 7 is depended on claim 6/5/1), Yasuho ('989)

discloses all of the limitations of the claimed invention, except for:

the connector terminals having four connector terminals each include: a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion;

the four connector terminals are each carried with the base portion attached to a transfer adapter and the four connector terminals are connected through soldering onto a rear surface of the board while attached to the transfer adapter.

Yasuho et al. ('402) shows an insulating substrate (7) comprising: four connector terminals (4) each include; a narrow, elongated base portion (frame 3) constituted of resin (column 4, lines 13-14); a plurality of pins (terminal pins 4) fixed to the base portion (3); the four connector terminals (4) are each carried with the base portion (3) attached to a transfer adapter (element 12-figures 1-2 or element 34-figure 22) and the four connector terminals are connected through soldering (column 4, lines 20-21) onto a rear surface of the board while attached to the transfer adapter (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. ('402) employed in the device of Yasuho ('989) in order to provide a high density electrical connection between board to board, heat dissipation from the component mounted on the board/substrate, and prevent an electromagnetic shield.

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Regarding claims 8 (claim 8 is depended on claim 6/5/1), Yasuho ('989)

discloses all of the limitations of the claimed invention, except for:

the four connector terminals each include: a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion; aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

Yasuho et al. ('402) shows an insulating substrate (7) having four connector terminals (4) each include; a narrow, elongated base portion (frame 3) constituted of resin (column 4, lines 13-14); a plurality of pins (terminal pins 4) fixed to the base portion (3);

aligning pins (14) projecting at both ends of the base portion (3) to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces (the inclined surfaces formed between the frame 3 and pin 14) for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes (the holes 13 of the element 12, figure 1) at which the aligning pins (14) are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals (14) are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. ('402) employed in the device of Yasuho (989) in order to provide a high density electrical connection between board to board, heat dissipation from the component mounted on the board/substrate, and prevent an electromagnetic shield.

Regarding claim 9, Yasuho ('989)) discloses a multilayer module board (element 7-figure 1, column 2, line 18) comprising:

a plurality of high-frequency electronic components (8, 10, 11, and 14, see column 2, lines 24-36) including at least one CPU (CPU-8, column 2, line 24) and a plurality of memory chips (**cache memory 11 and 14 data buffer LSI**);

the plurality of high-frequency electronic components (8, 10-11, 14) are electrically connected with one another through a wiring patterns (not shown) formed at an inner layer thereof (see column 1, lines 40-46); the multilayer module board (7) having shaped, which is a rectangular.

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Yasuho discloses all of the limitations of the claimed invention, except for:

connector terminals having four connector terminals provided as separate members each soldered onto one of four peripheral edges thereof;

the four connector terminals each include: a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion;

after the four connector terminals are each carried with the base portion attached to a transfer adapter and the four connector terminals are connected through soldering onto a rear surface of the board while attached to the transfer adapter.

Yasuho et al. ('402) shows an insulating substrate (7) comprising: connector terminals (4) having four connector terminals provided as separate members each soldered onto one of four peripheral edges (edges of a frame 3 of the substrate 7);

the four connector terminals (4) each include; a narrow, elongated base portion (frame 3) constituted of resin (column 4, lines 13-14); a plurality of pins (terminal pins 4) fixed to the base portion (3); the four connector terminals (4) are each carried with the base portion (3) attached to a transfer adapter (element 12-figures 1-2 or element 34-figure 22) and the four connector terminals are connected through soldering (column 4, lines 20-21) onto a rear surface of the board while attached to the transfer adapter (12).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. ('402) employed in the device of Yasuho ('989) in order to provide a high density electrical connection between board to board, heat dissipation

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from the component mounted on the board/substrate, and prevent an electromagnetic shield.

Regarding claim 10, Yasuho ('989)) discloses a multilayer module board (element 7-figure 1, column 2, line 18) comprising:

a plurality of high-frequency electronic components (8, 10, 11, and 14, see column 2, lines 24-36) including at least one CPU (CPU-8, column 2, line 24) and a plurality of memory chips (cache memory 11 and 14 data buffer LSI);

the plurality of high-frequency electronic components (8, 10-11, 14) are electrically connected with one another through a wiring patterns (not shown) formed at an inner layer thereof (see column 1, lines 40-46); the multilayer module board (7) having shaped, which is a rectangular.

Yasuho ('989) discloses all of the limitations of the claimed invention, except for: connector terminals having four connector terminals provided as separate members each soldered onto one of four peripheral edges thereof;

the four connector terminals each include: a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion; aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals are

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controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

Yasuho et al. ('402) shows an insulating substrate (7) having four connector terminals (4) each include; a narrow, elongated base portion (frame 3) constituted of resin (column 4, lines 13-14); a plurality of pins (terminal pins 4) fixed to the base portion (3);

aligning pins (14) projecting at both ends of the base portion (3) to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces (the inclined surfaces formed between the frame 3 and pin 14) for position control formed at both ends of the base portion to be used when soldering the connector terminal;

a pair of positioning holes (the holes 13 of the element 12, figure 1) at which the aligning pins (14) are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals (14) are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. ('402) employed in the device of Yasuho (989) in order to provide a high density electrical connection between board to board, heat dissipation

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from the component mounted on the board/substrate, and prevent an electromagnetic shield.

Response to Arguments

8. Appellant's arguments with respect to claims 1, 3, and 5-10 have been considered but are moot in view of the new ground(s) of rejection as explained below.

In the Reply Brief filed on 09/24/08:

Appellant argued:

a) Khosrowpour does not disclose, expressly or inherently, a multilayer module board including at least a CPU and a memory. (App. Br. 8).

Examiner acknowledges that in figure 1 of Khosrowpour, CPU and a memory is missing or **not labeled** a big chip and small chips as indicate as a CPU or memory chips mounted on a daughter board 102, and the daughter board 102 is not address as a multilayer circuit board.

However, in a new ground rejection as above, Yasuho ('989) discloses a circuit wiring board, which is a multilayer circuit module board (**element 7**-figure 1, column 2, line 18) having a plurality of high-frequency electronic components (**8, 10, 11, and 14**, see column 2, lines 24-36) including at least one CPU (**CPU-8**, column 2, line 24) and a plurality of memory chip (**catch memory 11 and 14 data buffer LSI**).

Further, Yasuho ('989) discloses the type of claimed multilayer module board, which is "one of a low-end module board, a high-speed module board or an

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advanced function module board" as explained in the rejection above (having a high-speed module board).

Therefore, examiner believes the Yasuho ('989) meets all of the limitations as claimed in claim 1 as shown above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lee Jinhee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/
Primary Examiner, Art Unit 2841.

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